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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/945,084	08/30/2001	Rich Fogal	2001-0128.00	3141
7590	12/23/2004		EXAMINER NGUYEN, KHIEM D	
Kevin D. Martin Agent for Applicant Micron Technology, Inc. 8000 S. Federal Way, MS 525 Boise, ID 83716			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/945,084

Applicant(s)

FOGAL ET AL.

Examiner

Khiem D Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 33-46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 33-46 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***New Grounds of Rejection***

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 33-35, 37-40, and 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over (JP 6-232537).

In re claim 33, **JP 6-232537** discloses a method of manufacturing a semiconductor device, comprising: forming a first circuit (FIGS. 3a-c: 11, located on the left side) and a second circuit (FIGS. 3a-c: 11, located on the right side) on a semiconductor wafer substrate assembly; forming a first conductor connected to the first semiconductor circuit and a second conductor connected to the second semiconductor circuit (JP 6-232537 English translation, page 1, paragraph [0005] and FIGS. 3a-c), wherein the first conductor is electrically separated from the second conductor such that the first and second circuits are sufficiently isolated to provide protection to the second circuit (FIGS. 3a-c); with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other (English translation, pages 1-2); subsequent to performing the electrical operation on the first circuit, shorting the first and second

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conductors together to electrically couple the first and second circuits (FIGS. 3b-c); and subsequent to shorting the first and second conductors together (FIGS. 3c: 14), encapsulating the semiconductor wafer substrate assembly (JP 6-232537 English translation, pages 1-2 and FIGS. 1-3). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to perform an electrical operation on the first circuit with a voltage sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other because the disclose process would required the same functional limitations as cited in the Applicants' claimed invention since the same materials are treated in the same manner as in the instant invention (MPEP § 2173.05(g)).

A functional limitation is an attempt to define something by what it does, rather than by what it is (e.g., as evidenced by its specific structure or specific ingredients). There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. *In re Swinshart*, 439 F.2d 210, 169 USPQ 226 (CCPA 1971).

A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in association with an element, ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step. Whether or not the functional limitation complies with 35 U.S.C. 112, second paragraph, is a different issue from whether the limitation is properly supported under 35 U.S.C. 112, first paragraph, or is distinguished over the prior art. A few examples are set forth below to illustrate situations where the issue of whether a functional limitation complies with 35 U.S.C. 112, second paragraph, was considered.

It was held that the limitation used to define a radical on a chemical compound as "incapable of forming a dye with said oxidizing developing agent" although functional, was perfectly acceptable because it set definite boundaries on the patent protection sought. *In re Barr*, 444 F.2d 588, 170 USPO 33 (CCPA 1971).

In re claim 34, JP 6-232537 discloses wherein the method of claim 33 further comprising shorting the first and second conductor together with a ball bond (FIG. 3c: 14) (English translation, page 1, paragraph [0005]).

In re claim 35, JP 6-232537 discloses wherein the first and second circuits are fabricated such that the memory device is inoperative if the first and second conductors remain electrically separate subsequent to encapsulation (English translation, pages 1-2 and FIGS. 1-3).

In re claim 37, JP 6-232537 discloses a method of manufacturing a memory device, comprising: forming a plurality of primary and redundant memory cell locations; forming antifuse circuitry which allows selection of the redundant memory cell locations; forming voltage sensitive circuitry on the semiconductor wafer substrate assembly; forming a first conductor (FIGS. 3a-c: 11 located on the left side) electrically connected with the antifuse circuitry; forming a second conductor (FIGS. 3a-c: 11 located on the right side) electrically connected with the voltage sensitive circuitry, wherein the first and second conductors are electrically separated from each other (FIG. 3a); while the first and second conductors are electrically separated, applying a voltage to the antifuse circuitry to program the antifuse circuitry, wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected (English translation, pages 1-2); and subsequent to programming the antifuse circuitry, electrically shorting the first conductor with the second conductor (FIG. 3c: 14) (English translation, page 1, paragraph [0005]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a voltage to the antifuse circuitry to program the antifuse circuitry, wherein the voltage is sufficient to damage the voltage sensitive circuitry when applied to the antifuse circuitry when the first and second conductors are electrically connected because the

disclose process would required the same functional limitations as cited in the Applicants' claimed invention since the same materials are treated in the same manner as in the instant invention (MPEP § 2173.05(g)).

In re claim 38, **JP 6-232537** discloses wherein the method of claim 37 further comprising encapsulating the antifuse circuitry, the voltage sensitive circuitry, the first conductor, and the second conductor subsequent to electrically shorting the first conductor with the second conductor (English translation, page 2).

In re claim 39, **JP 6-232536** discloses wherein the method of claim 37 further comprising electrically shorting the first conductor with the second conductor using a ball bond (FIG. 3c: 14) (English translation, page 1, paragraph [0005]).

In re claim 40, **JP 6-232536** discloses wherein the antifuse circuitry and the voltage sensitive circuitry are fabricated such that the memory device is inoperative if the first and second conductors remain electrically separated (English translation, pages 1-2 and FIGS. 1-3).

In re claim 42, **JP 6-232537** discloses a method of manufacturing a memory device comprising: fabricating first and second circuits on a semiconductor wafer substrate assembly, wherein the first and second circuits are adapted to be electrically connected through a common conductor 11 (FIGS. 3a-c); fabricating the common conductor with a physical opening to provide an open circuit (predetermined gap) between the first and second circuits (English translation, page 1, paragraph [0005] and FIG. 3a), such that the first circuit is sufficiently isolated from the second circuit to provide protection for the first circuit from a voltage applied to the second circuit which

is sufficient to damage the first circuit when applied to the second circuit with the physical opening bridged (English translation, page 1, paragraph [0005]); applying the voltage to the second circuit; and subsequent to applying the voltage to the second circuit, bridging the physical opening of the common conductor to electrically connect the first and second circuits together (FIG. 3c: 14) (English translation, page 1, paragraph [0005]). It would have been obvious to one of ordinary skill in the art at the time of the invention was made that the first circuit is sufficiently isolated from the second circuit to provide protection for the first circuit from a voltage applied to the second circuit which is sufficient to damage the first circuit when applied to the second circuit with the physical opening bridged because the disclose process would obtain the same functional limitations as cited in the Applicants' claimed invention since the same materials are treated in the same manner as in the instant invention (MPEP § 2173.05(g)).

In re claim 43, **JP 6-232537** discloses wherein the method of claim 42 further comprising encapsulating the first and second circuits and the common conductor subsequent to bridging the physical opening (English translation, page 2).

In re claim 44, **JP 6-232536** discloses wherein the method of claim 42 further comprising bridging the physical opening with a ball bond (FIG. 3c: 14) (English translation, page 1, paragraph [0005]).

In re claim 45, **JP 6-232536** discloses wherein the first and second circuits are fabricated such that the memory device is inoperative if the physical opening remains unbridged (English translation, pages 1-2 and FIGS. 1-3).

2. Claims 36, 41, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over (JP 6-232537) in view of the applicant's admitted prior art (AAPA) of this application.

In re claims 36, 41, and 46, AAPA discloses providing a lead frame, and subsequent to shorting the first and second conductors together, attaching the semiconductor wafer substrate assembly to the lead frame (page 4, paragraph [0010]). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of JP 6-232537 and AAPA in such a way that the lead frame and die are encapsulated or otherwise packaged (page 4, paragraph [0010]).

***Response to Applicants' Amendment and Arguments***

Applicant's arguments with respect to claims 33-46 have been considered but are moot in view of the new ground(s) of rejection.

Applicants contend that the translation of JP 6-232537 does not teach that a voltage is applied to the resistor in order to trim the resistor.

In response to Applicants' contention that the translation of JP 6-232537 does not disclose that a voltage is applied sufficient to damage the second circuit when applied to the first circuit with the first and second circuits electrically connected to each other, Examiner respectfully disagrees. Since Applicants' amendment necessitated the new ground(s) of rejection presented in this Office Action, Applicants' argument is moot. For this reason, Examiner holds the rejection proper.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §



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706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

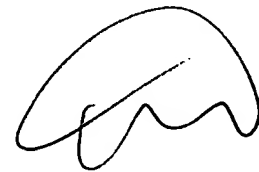
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.  
December 17<sup>th</sup>, 2004

A handwritten signature in black ink, appearing to read 'W. David Coleman', with a large, sweeping initial 'W'.

**W. DAVID COLEMAN  
PRIMARY EXAMINER**